Dr. Öğr. Üyesi BURAK ÜNAL

Kişisel Bilgiler

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Biyografi

Dr. Burak Ünal received the B.Sc. degree (Hons.) in Electrical and Electronics Engineering from Erciyes University, Kayseri, Turkey, in 2008, the M.Sc. and Ph.D. degree in Electrical and Computer Engineering from the University of Arizona, Tucson, AZ, USA, in 2013, and 2019. His current research interests include design, development, and analysis of low-complexity iterative decoding algorithms for error correction codes (low-density parity check) and their efficient hardware architectures.

Eğitim Bilgileri

Bütünleşik Doktora, The University of Arizona, Faculty of Engineering , Department of Electrical and Computer Engineering, Amerika Birleşik Devletleri 2013 - 2019

Verdiği Dersler

Digital Design , Lisans, 2023 - 2024, 2022 - 2023, 2021 - 2022, 2020 - 2021
High Performance Computing, Yüksek Lisans, 2023 - 2024, 2022 - 2023
System on Chip Design, Lisans, 2024 - 2025, 2023 - 2024, 2022 - 2023

SCI, SSCI ve AHCI İndekslerine Giren Dergilerde Yayınlanan Makaleler

I. **Hardware Implementation and Performance Analysis of Resource Efficient Probabilistic Hard Decision LDPC Decoders**
ÜNAL B., Akoglu A., Ghaffari F., Vasic B.
IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I-REGULAR PAPERS, cilt.65, sa.9, ss.3074-3084, 2018 (SCI-Expanded)

Hakemli Kongre / Sempozyum Bildiri Kitaplarında Yer Alan Yayınlar

I. **Design of High Throughput FPGA-Based Testbed for Accelerating Error Characterization of LDPC Codes**
Unal B., Hassan M. S., Mack J., Kumbhare N., Akoglu A.
2019 International Conference on Reconfigurable Computing and FPGAs, ReConFig 2019, Cancun, Meksika, 9 - 11

Aralık 2019

II. **Accelerated Shadow Detection and Removal Method**
Richter E., Raettig R., Mack J., Valancius S., Unal B., Akoglu A.
16th IEEE/ACS International Conference on Computer Systems and Applications (AICCSA), Abu Dhabi, Birleşik Arap Emirlikleri, 3 - 07 Kasım 2019

III. **Efficient FPGA implementation of probabilistic gallager B LDPC decoder**
Ghaffari F., ÜNAL B., Akoglu A., Le K., Declercq D., Vasic B.
2017 24th IEEE International Conference on Electronics, Circuits and Systems (ICECS), Batumi, Gürcistan, 5 - 08 Aralık 2017

IV. **Analysis and implementation of resource efficient probabilistic Gallager B LDPC decoder**
ÜNAL B., Ghaffari F., Akoglu A., Vasic B., Declercq D.
2017 15th IEEE International New Circuits and Systems Conference (NEWCAS), Strasbourg, France, 25 - 28 Haziran 2017

V. **Resource efficient real-time processing of Contrast Limited Adaptive Histogram Equalization**
ÜNAL B., Akoglu A.
2016 26th International Conference on Field Programmable Logic and Applications (FPL), Lausanne, Switzerland, 29 Ağustos - 02 Eylül 2016

Desteklenen Projeler

Ünal B., Baran A., TÜBİTAK Projesi, 5G YENİ RADYO UYUMLU LDPC TABANLI FİZİKSEL KATMAN İLERİ HATA DÜZELTME IP ÇEKİRDEK GELİŞTİRME, 2021 - 2023

Metrikler

Yayın: 6
Atıf (WoS): 6
Atıf (Scopus): 13
H-İndeks (WoS): 1
H-İndeks (Scopus): 1